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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new non-provisional applications under 37 CFR 1.53(b))

Attorney Docket No.	*94-0302.02*	*Total Pages*	
First Named Inventor or Application Identifier			
Thakur			
Express Mail Label No.	*EL003000565US*		

jc867 U.S. PTO 08/31/00

jc474 U.S. PTO 09/654093 08/31/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification *Total Pages 17 (preferred arrangement set forth below)*
-Descriptive
-Cross References to Related Application
-Statement Regarding Fed sponsored R & D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings *(if filed)*
-Detailed Description
-Claim(s)
-Abstract of the Disclosure

3. ☒ Drawing(s) *(35 USC 113)* *Total Sheets 2* *Total Pages 6*

4. Oath or Declaration
a. ☐ Newly executed (original or copy)
b. ☒ Copy from a prior application (37CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))

9. ☒ 37 CFR 3.73(b) Statement ☒ Power of Attorney *(where there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)

14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application Status still proper and desired

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Other

17. ☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: ____/_____

18. CORRESPONDENCE ADDRESS

☐ *Customer Number or Bar Code Label* ☐ *Correspondence address below*

(Insert Customer No. or Attach bar code label here)

NAME	Charles Brantley				
	Micron Technology, Inc.				
ADDRESS	8000 S. Federal Way				
	Mail Stop 525				
CITY	Boise	*STATE*	Idaho	*ZIP CODE*	83716
COUNTRY	USA	*TELEPHONE*	(208) 368-4557	*Fax*	(208) 368-5606

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Randhir Thakur, Ravi Iyer, and Howard Rhodes	§	
	§	Group Art Unit:
Serial No.:	§	
	§	Examiner:
Filed: August 31, 2000	§	
	§	Atty. Docket: 94-0302.02
For: A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS	§	
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PRELIMINARY AMENDMENT

Assistant Commissioner for Patents

Washington, D.C. 20231

"EXPRESS MAIL" MAILING LABEL NoEL003000565US
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I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R. § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.
Trish Howard Stoller
Signature

Dear Sir:

After awarding the above-captioned application the benefit of the priority date of its grandparent -- application #08/578,825, filed December 26, 1995-- please amend the current application as follows.

IN THE SPECIFICATION:

Immediately after the title, please add the following: --

Related Applications

This application is a divisional of pending U.S. Application Ser. No. 09/312,373, filed May 13, 1999; which is a continuation of U.S. Application Ser. No. 08/578,825 filed Dec. 26, 1995, now abandoned. --

On page 7, line 19, please replace "tetraethylorthophosphate" with -- triethylphosphate --.

On page 9, line 26, please replace "silane oxide" with -- silane-based oxide --.

Also on page 9, line 26, please replace "silane oxynitride" with -- silane-based oxynitride --.

On page 9, line 29, please replace "silane" with -- silane-based --.

On page 9, line 30, please replace "silane oxide" with -- silane-based oxide --.

IN THE CLAIMS

Please amend the claims as follows.

Please cancel claims 1-35 without prejudice.

Please add the following claims:

36. A semiconductor device, comprising:

an electrically conductive member;

a dielectric layer under said conductive member, said dielectric layer containing a dopant and a contaminant;

a contaminant barrier under said dielectric layer;

an insulating region under said contaminant barrier; and

a plurality of electrically conductive regions under said contaminant barrier and flanking said insulating region.

37. The semiconductor device in claim 36, wherein said contaminant barrier comprises at least one material selected from an oxide, an oxynitride, a nitride, and combinations thereof.

38. The semiconductor device in claim 37, wherein said contaminant barrier comprises at least two materials selected from an oxide, an oxynitride, a nitride, and combinations thereof.

39. The semiconductor device in claim 37, wherein said electrically conductive member comprises a lead.

40. A circuit device, comprising:

a conductive structure configured to receive a voltage;

a first insulation portion under said conductive structure, said first insulation portion including an organic contaminant;

a second insulation portion under said first insulation portion, said second insulation portion having an index of refraction ranging from 1.5 to 2.6; and

a substrate under said second insulation portion and comprising:

an electrically conductive first region,

an electrically conductive second region, and

an insulation region between said first region and said second region.

41. The circuit device in claim 40, wherein said first region is a first active area within a well; and said second region is a second active area within said well.

42. The circuit device in claim 40, wherein said first region is a first well and said second region is a second well.

43. The circuit device in claim 40, wherein said first region is a first n-well and said second region is a second n-well.

44. An insulative stack between a top conductive member and a lower-lying plurality of conductive areas, said insulative stack comprising:

an insulating region between said plurality of conductive areas;

a carbon barrier over said insulating region; and

a carbon-containing dielectric over said carbon barrier and under said top conductive member.

45. The insulative stack in claim 44, wherein said insulating region comprises a field oxide.

46. The insulative stack in claim 44, wherein said insulating region comprises a trench oxide.

47. A barrier between a dielectric contaminated with an electrically chargeable material and an insulating region generally free of said electrically chargeable material, said barrier comprising insulation for an integrated circuit device, wherein said insulation defines a first interface with said dielectric and a second interface with said insulating region; and wherein said first interface has a first concentration of said electrically chargeable material that is greater than a second concentration of said electrically chargeable material at said second interface.

48. The barrier in claim 47, wherein said insulation comprises aluminum oxide.

49. The barrier in claim 47, wherein said insulation comprises aluminum nitride.

50. The barrier in claim 47, wherein said insulation has a thickness ranging from 50 Angstroms to 2000 Angstroms.

51. The barrier in claim 50, wherein said insulation has a thickness ranging from 100 Angstroms to 1000 Angstroms.

52. A method of processing a semiconductor device, comprising:
depositing a dielectric layer over a semiconductor substrate;
allowing electrically chargeable particles to occur in said dielectric layer;
allowing some diffusion of said electrically chargeable particles; and
preventing at least some of said electrically chargeable particles from reaching said substrate.

53. The method in claim 52, wherein:
said step of depositing a dielectric layer comprises depositing a dielectric layer using a organic precursor;
said step of allowing electrically chargeable particles to occur in said dielectric layer comprises allowing an organic component of said organic precursor to deposit in said dielectric layer; and

said preventing step comprises layering a barrier over said substrate using a non-organic precursor prior to said step of depositing a dielectric layer.

54. The method in claim 53, wherein said layering step comprises layering a barrier using silane.

55. A method of at least partially forming a circuit device, comprising:

providing a semiconductor substrate;

layering a carbon-free barrier on said substrate; and

layering a carbon-containing dielectric on said barrier.

56. The method in claim 55, wherein said step of layering a carbon-free barrier on said substrate further comprises layering said carbon-free barrier using a plasma.

57. The method in claim 56, further comprising a step of heating said carbon-containing dielectric.

58. The method in claim 57, wherein said step of heating said carbon-containing dielectric comprises raising a temperature of said dielectric to a range of 850° C to 1050° C for at least 5 seconds.

59. The method in claim 57, wherein said step of heating said carbon-containing dielectric comprises raising a temperature of said dielectric to a range of 750° C to 1000° C for at least 5 minutes.

60. A method of processing a substrate comprising two active areas and an intervening insulating region, said method comprising:

depositing an oxide charge barrier over said substrate;

depositing a generally insulative material over said oxide charge barrier, wherein said generally insulative material is less insulative than said barrier; and

providing a generally conductive element over said generally insulative material,

wherein said element is generally laterally coextensive with said intervening insulating region.

61. The method in claim 60, wherein said step of depositing a generally insulative material comprises depositing a generally insulative material that is allowed to comprise oxide charges.

62. The method in claim 61, further comprising a step of plasma treating said substrate prior to said step of depositing an oxide charge barrier.

63. The method in claim 61, further comprising:

annealing said generally insulative material;

allowing an oxide charge in said generally insulative material to migrate toward said substrate in response to said annealing step; and

intercepting said oxide charge with said oxide charge barrier before said oxide charge reaches said substrate.

64. The method in claim 61, further comprising refraining from depositing any generally conductive material before said step of depositing a generally insulative material.

Please cancel claims 36-51 without prejudice.

REMARKS

Claims 52-64 are the only claims pending as of this Preliminary Amendment. Per a telephone conversation held with the Examiner of the parent application on July 19, 1999, Applicants elected to pursue the device claims (claims 36-51) during prosecution of that application. Accordingly, Applicants seek to pursue the method claims (52-64) in this divisional application. If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is requested to contact Applicants' undersigned attorney at the number indicated.

Respectfully submitted,

Date: 8/31/00

Charles Brantley

Charles B. Brantley II
Reg. No. 38,086
Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83706-9632
(208) 368-4557
ATTORNEY FOR APPLICANTS

09575800 - 083100

Micron Docket No. 94-0302

Micron Technology, Inc.

A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS

Background of the Invention

1. Field of the Invention

This invention relates to integrated circuit structures, and in particular, it relates to dielectric materials used within dynamic random access memory cells formed on semiconductor integrated circuits.

2. Background Art

In a conventional transistor a gate is separated from the source and drain by a dielectric layer. When a sufficient voltage level is applied to the gate the transistor turns on and current flows between the source and the drain of the transistor. In a similar manner, when conductors of integrated

circuits pass over dielectric layers located above adjacent n-wells or diffusion regions they can cause leakage current to flow between the n-wells or between the diffusion regions. This leakage current is very undesirable.

It is well known in the art of semiconductor fabrication that dielectric layers formed from organic sources can have shifts in their threshold voltage due to impurities in the dielectric material. The impurities are present in the layer because of the organic processes, such as ozone-TEOS based chemistry, which are used to form the material of the dielectric layer.

It is also known for the impurities in the dielectric layer to diffuse and collect at interfaces close to the substrate during high temperature processing steps performed after deposition of dielectric material formed with organometallic precursors. This diffusion can seriously degrade integrated circuit operation.

It is therefore an object of the present invention to provide a process for forming dielectric material for semiconductor fabrication using organic chemistry such as ozone-TEOS based chemistry and organometallic precursors which leave undesirable impurities in the dielectric material.

It is a further object of the present invention to eliminate or reduce threshold voltage shift caused by impurities that are a consequence of the organic processes for forming the dielectric layer.

It is a further object of the present invention to provide such a process for BPSG films that are thicker than at least 5KA.

It is a further object of the present invention to prevent the problems associated with diffusion of impurities in dielectric layers to interfaces near the surface of the substrate.

These and other objects and advantages of the invention will become more fully apparent from the description and claims which follow or may be learned by the practice of the invention.

Summary of the Invention

A method of fabricating an integrated circuit having reduced threshold voltage shift is provided. A nonconducting region is formed on the semiconductor substrate and active regions are formed on the semiconductor substrate. The active regions are separated by the nonconducting region. A barrier layer and a dielectric layer are deposited over the nonconducting region and over the active regions. Heat is applied to the integrated circuit causing the barrier layer to anneal. The dielectric layer can be a BPSG film. Preferably BPSG films are deposited using organometallic precursors. More specifically, ozone (4 to 20% vol conc.), TEOS, TEPO (as an example of a P source) and TEB (as an example of a B source) are reacted at a temperature of at least 300°C such that BPSG films of at least one thousand angstroms are formed at a deposition rate in the range of 500 angstroms/min to 6000 angstroms/min using gas or liquid injection for carrying the species into the reaction

chamber. The preferred deposition temperature range is 300°C - 600°C. The deposition may be done at atmospheric or subatmospheric pressure, in a plasma or a non-plasma based reactor and deposition conditions and the dopant concentration can be varied to obtain the desired film properties and composition. Hot wall reactors can also be used for BPSG film deposition.

Brief Description of the Drawings

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained can be appreciated, a more particular description of the invention briefly described above will be rendered by reference to a specific embodiment thereof which is illustrated in the appended drawings. Understanding that these drawings depict only a typical embodiment of the invention and are not therefore to be considered limiting of its scope, the invention and the presently understood best mode thereof are described and explained with additional specificity and detail through the use of the accompanying drawings.

Fig. 1 shows a cross-sectional schematic representation of a prior art semiconductor integrated circuit which may be used in accordance with the method of the present invention.

Fig. 2 shows a graphical representation of the threshold voltage shift in integrated circuits that is solved by the method of the present invention.

Fig. 3 shows a cross-sectional schematic representation of the semiconductor integrated circuit of Fig. 1 including a barrier layer formed in accordance with the method and structure of the present invention.

Detailed Description of the Invention

Referring now to Fig. 1, there is shown a prior art cross-sectional representation of a semiconductor device 10. Active regions 12 are formed within a silicon layer 18. It will be understood by those skilled in the art that the active regions 12 can be any type of diffused regions such as n+, p+, n-, or p- regions or collections of transistors formed within n-wells or p-wells. The active regions 12 are separated from each other by an insulating region 14. It will also be understood by those skilled in the art that the insulating region 14 spacing the active regions apart may be, for example, a field oxide region between two diffusion regions, a trench oxide or any other type of isolating region. Thus, region 14 can be any kind of insulating region between active areas within an n-well or a p-well. A dielectric layer 20 is deposited over the active regions 12 and the field oxide layer 14. The dielectric layer 20 can be formed of, for example, BPSG, BSG, PSG or silicon dioxide. A lead 26 is located above the dielectric layer 20. During use of an integrated circuit formed with the semiconductor device 10 a voltage level on the lead 26 may give rise to a small leakage current 16 between the active regions 12 under the insulating region 14.

Leakage current 16 between isolated active areas in a p-well or an n-well is enhanced by the presence of oxide charges 24 within the dielectric layer 20 upon application of a voltage to lead 26. While oxide charges 24 are indicated with "+" in the drawings for illustrative purposes, it will be understood that oxide charges 24 can be positive or negative. For example, negative charges can be present with an n-well structure and positive charges can be present with a p-well structure. Thus, the leakage current between active areas in an n-well structure is enhanced by the presence of negative oxide charges. If additional oxide charges 24 are present in the dielectric layer 20 the problems associated with oxide charges 24 increase. Thus, when the dielectric layer 20 is formed with a greater thickness, the problems are increased due to the greater amount of oxide charges 24 that are carried by the additional BPSG or other material of the thicker dielectric layer 20. The oxide charges 24 are a substantial problem for thicknesses over one thousand angstroms.

Referring now to Fig. 2, there is shown a graphical representation 50 for a p-type substrate 18. The graphical representation 50 illustrates the relationship between the voltage applied to the lead 26 and the capacitance in the dielectric layer 20. If there is no oxide charge 24 in the dielectric layer 20 the curve 54 results. If positive charges 24 are present in the dielectric layer 20 the flatband shift of curve 52 results. If negative charges 24 are present in the dielectric layer 20 the flatband shift of curve 56 results.

The primary source of the oxide charges 24 present within the dielectric layer 20 is contamination of the dielectric layer 20. One of the potential sources of the contamination in the dielectric layer 20 can be carbon. The contamination of the layer 20 occurs during production of the BPSG or other type of material forming layer 20. It is well understood that molecules acting as sources of boron, phosphorous and silicon atoms must react with oxygen in order to form the BPSG, BSG, PSG or other material of the dielectric layer 20. The contamination of the dielectric layer 20 can thus occur due to the use of organometallic precursors that can be used to provide the boron, phosphorus, silicon and oxygen atoms of the BPSG of the dielectric layer 20.

For example it is known to form the BPSG material of the dielectric layer 20 by reacting ozone with organic precursors such as $(C_2H_5O)_4Si$ (TEOS) tetraethylorthophosphate (TEPO) and triethylborane (TEB) in order to provide the required boron, phosphorous, and silicon atoms. Each of these molecules is an organic molecule containing carbon atoms. The contamination due to the carbon of the organic molecules remains in the BPSG dielectric layer 20 after the reactions forming the BPSG material and cause impurities in the BPSG layer 20. Furthermore, it will be understood that contamination can arise in any other way from the organic precursors and from any other sources. For example, impurities mixed with the organic precursors can cause the contamination. The contamination causes the oxide charges 24 to be present

in the dielectric layer 20 and, thereby, causes threshold voltage shift. Other contamination sources can also be present that would give rise to charged regions in oxide.

It is also known in the prior art to obtain the boron, phosphorus and silicon atoms required for forming the BPSG or other material of the dielectric layer 20 from sources that are not organic sources and do not contaminate the layer 20 in this manner. For example, either in the presence of a plasma or at atmospheric pressure, oxygen may be reacted with silane (SiH_4), phosphine (PH_3) and/or diborane (B_2H_6) in order to form BPSG.

However, the use of organometallic precursors such as TEOS, TEPO and TEB to form dielectric materials for semiconductor fabrication is preferred to the use of the inorganic materials for several reasons. The organic reactions permit better control of the fabrication process. For example, the organic reactions provide more precise control of doping and oxide thickness. Furthermore, they permit better step coverage.

Referring now to Fig. 3, there is shown a cross-sectional representation of a semiconductor device 100 formed in accordance with a preferred method of the present invention. The semiconductor device 100 is substantially similar to the semiconductor device 10 except for the addition of a barrier layer 30. The barrier layer 30, is deposited below the dielectric layer 20 and above the active regions 12 and the insulating region 14.

The depositing of layer 20 can be followed by heating the layer 20 to at least 550°C. In one preferred embodiment rapid thermal processing is performed. In rapid thermal processing, the temperature of layers 20 and 30 is raised to between approximately 850°C and 1050°C for at least five seconds causing the layer 20 to reflow. In another preferred embodiment the temperature can be raised to approximately 750°C to 1000°C in a furnace for at least five minutes. During the reflow of the dielectric layer 20, and during any other subsequent high temperature process steps which may occur, the impurities within the dielectric layer 20 may diffuse. For example, without the barrier layer 30 the impurities may diffuse to the interface between the dielectric layer 20 and the active regions 12 and, more likely, to the interface between the dielectric layer 20 and the insulating region 14 and degrade the performance of the integrated circuit. The barrier layer 30 blocks diffusion of the impurities into the active regions 12 and into the insulating region 14 during the reflow step and/or any other high temperature process steps.

The barrier layer 30 can be formed in many different ways. For example, the barrier layer 30 can be a silane oxide layer or a silane oxynitride layer. Additionally, the barrier layer 30 can be a nitride film which can be formed using plasma technology or using non-plasma technology. Additionally, silane nitride or nitride with a silane oxide stack can be used. Additionally, the layer 30 can be a composite layer formed of layers of silicon dioxide and silicon nitride. Thus, in accordance with the present invention the organic dielectric layer 20 is deposited

over any of these barrier layers 30 or barrier stacks 30. The barrier layer 30 formed in this manner can be in the range of approximately fifty angstroms to approximately two thousand angstroms. Preferably, it is between one-hundred and one-thousand angstroms.

Prior to depositing the barrier layer 30 and before forming any of the previously described stacks a plasma treatment of the semiconductor device 10 can be performed. The plasma treatment can be a conventional high voltage plasma treatment using oxygen plasma, ozone plasma, nitrogen plasma, ammonia plasma or a combination of the these gases.

It has been determined that the refractive index of materials can serve as an indication of whether they are suitable for forming the material of the barrier layer 30 of the present invention because the index of refraction of these materials is related to their nitrogen content. The range of satisfactory refractive indices for a material to function as the barrier layer 30 of the present invention is from approximately 1.5 to 2.6. The refractive index of silicon nitride is typically approximately 2.0. The refractive index of oxynitride is typically between approximately 1.46 and 2.0. The refractive index of silicon rich oxynitride is between approximately 2.0 and 2.6. The refractive index of silicon dioxide is approximately 1.46. The refractive index of a composite layer 30 formed of silicon dioxide and silicon nitride is somewhere between the indices of the silicon dioxide and silicon nitride depending on the relative amount of each material used in forming the layer. Although other barrier materials having a refractive index within the range can be used, it will

be understood that a material forming the barrier layer 30 must be structurally sound in addition to having a refractive index in this range. It is thus understood that many other materials can be used to form the layer 30. For example, aluminum oxide and aluminum nitride and other insulating materials can be used.

It is to be understood that although the present invention has been described with reference to a preferred embodiment, various modifications, known to those skilled in the art, may be made to the structures and process steps presented herein without departing from the invention as recited in the several claims appended hereto. For example, the use of the barrier layer 30 is taught under the lead 26 and over the active regions 12 and the insulating region 14. In one preferred embodiment, the barrier layer 30 of the present invention may be deposited above n-wells and/or p-wells wherein integrated circuit active regions are formed in the n-wells and/or p-wells in a conventional manner. It will be understood that the method of the present invention prevents n-well to n-well leakage and p-well to p-well leakage as well as preventing leakage between active regions within n-wells or p-wells. Furthermore, the method of the present invention may be used to prevent metal field leakage and poly field leakage in general.

CLAIMS

1. A method of fabricating an integrated circuit having a reduced threshold voltage shift in a semiconductor substrate, comprising the steps of:

(a) forming a nonconducting region upon said semiconductor substrate;

(b) forming active regions upon said semiconductor substrate wherein said active regions are separated by said nonconducting region;

(c) depositing a barrier layer over said nonconducting region and over said active regions;

(d) depositing a dielectric layer formed from an organic precursor; and

(e) heating said barrier layer and said dielectric layer to a temperature of at least 550° C.

2. The fabrication method of claim 1, wherein said barrier layer has a thickness of between approximately 50 angstroms and approximately 2,000 angstroms.

3. The fabrication method of claim 2, wherein said barrier layer has a thickness of between approximately 100 angstroms and approximately 1,000 angstroms.

4. The fabrication method of claim 1, wherein said active regions comprise transistor elements.

5. The fabrication method of claim 1, wherein said nonconducting region comprises a field oxide region.

6. The fabrication method of claim 1, wherein said nonconducting region comprises a trench between two active regions.

7. The fabrication method of claim 1, wherein said active regions are located within an n-well.

8. The fabrication method of claim 7, wherein a plurality of integrated circuit transistors is formed within said n-well.

9. The fabrication method of claim 1, wherein said active regions are located within a p-well.

10. The fabrication method of claim 9, wherein a plurality of integrated circuit transistors is formed within said p-well.

11. The fabrication method of claim 1, wherein said active regions are diffusion regions.

12. The fabrication method of claim 11, wherein a plurality of integrated circuit transistors is formed within said diffusion regions.

13. The fabrication method of claim 1, wherein said dielectric layer comprises a BPSG layer formed from an organic precursor.

14. The fabrication method of claim 1, wherein said dielectric layer comprises a BSG layer formed from an organic precursor.

15. The fabrication method of claim 1, wherein said dielectric layer comprises a PSG layer formed from an organic precursor.

16. The fabrication method of claim 13, comprising the further step of reacting a material selected from the group consisting of TEOS, TEPO and TEB to form said BPSG.

17. The fabrication method of claim 1, wherein said barrier layer comprises silane oxide.

18. The fabrication method of claim 1, wherein said barrier layer comprises silane oxynitride.

19. The fabrication method of claim 1, wherein said barrier layer comprises a nitride film.

20. The fabrication method of claim 1, wherein said barrier layer comprises a plasma nitride film.

21. The fabrication method of claim 1, wherein said barrier layer comprises silane nitride.

22. The fabrication method of claim 1, wherein said barrier layer comprises nitride with silane oxide deposited thereupon.

23. The fabrication method of claim 1, wherein said barrier layer comprises a composite film formed of silicon dioxide and silicon nitride layers.

24. The fabrication method of claim 1, wherein said barrier layer comprises layers of oxide with a nitride film therebetween.

25. The fabrication method of claim 13, comprising a further barrier layer deposited over said BPSG layer and a further BPSG layer deposited over said further barrier layer.

26. The fabrication method of claim 1, comprising the step of performing rapid thermal processing of said layers.

27. The fabrication method of claim 26, comprising the step of heating said barrier and dielectric layers to approximately between 850°C and 1050°C for at least five seconds.

28. The fabrication method of claim 1, comprising the step of heating said barrier and dielectric layers in a furnace to between approximately 750°C and approximately 1000°C for at least five minutes.

29. The fabrication method of claim 1, comprising the step of applying a plasma treatment to said semiconductor surface prior to performing step (c) and step (d).

30. The fabrication method of claim 29, comprising the step of applying a plasma selected from the group consisting of oxygen plasma, ozone plasma, nitrogen plasma and ammonia plasma.

31. The fabrication method of claim 30, comprising the step of applying a plurality of said plasmas of said group.

32. The fabrication method of claim 1, wherein said dielectric layer has a thickness greater than one thousand angstroms.

33. The fabrication method of claim 1, wherein said barrier layer comprises oxynitride having a refractive index between approximately 1.46 and 2.0.

34. The fabrication method of claim 1, wherein said barrier layer comprises silicon rich oxynitride having a refractive index between approximately 2.0 and 2.6.

35. The fabrication method of claim 29, further comprising the step of depositing a dielectric layer directly upon said plasma treated surface.

Abstract Of The Invention

A method of fabricating an integrated circuit having reduced threshold voltage shift is provided. A nonconducting region is formed on the semiconductor substrate and active regions are formed on the semiconductor substrate. The active regions are separated by the nonconducting region. A barrier layer and a dielectric layer are deposited over the nonconducting region and over the active regions. Heat is applied to the integrated circuit causing the barrier layer to anneal.

PRIOR ART

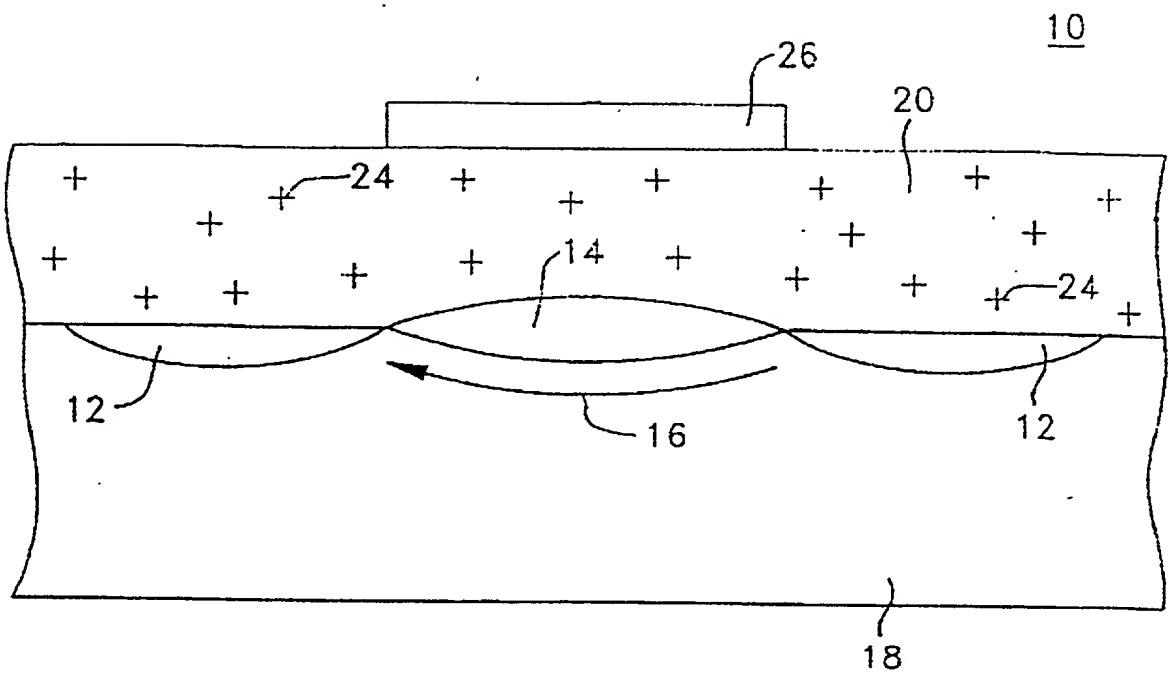

FIG. 1

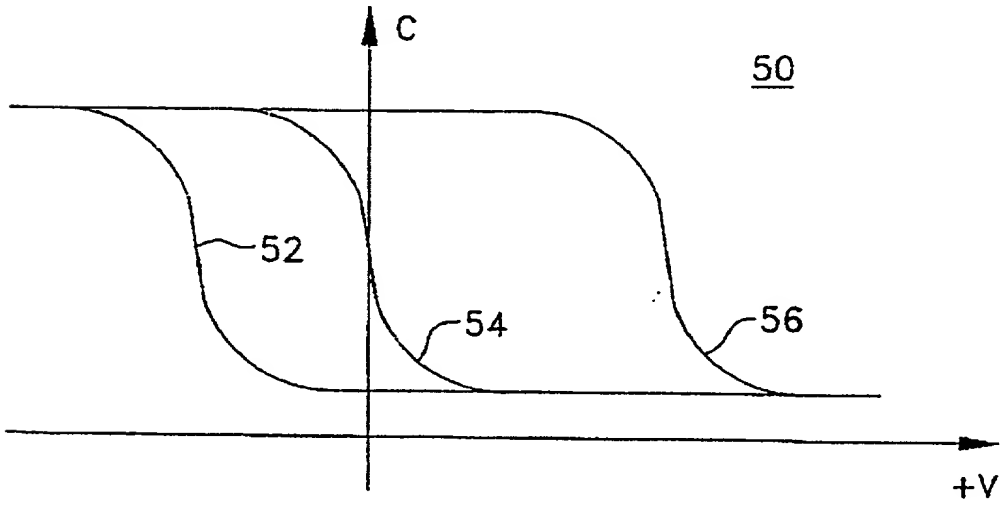

FIG. 2

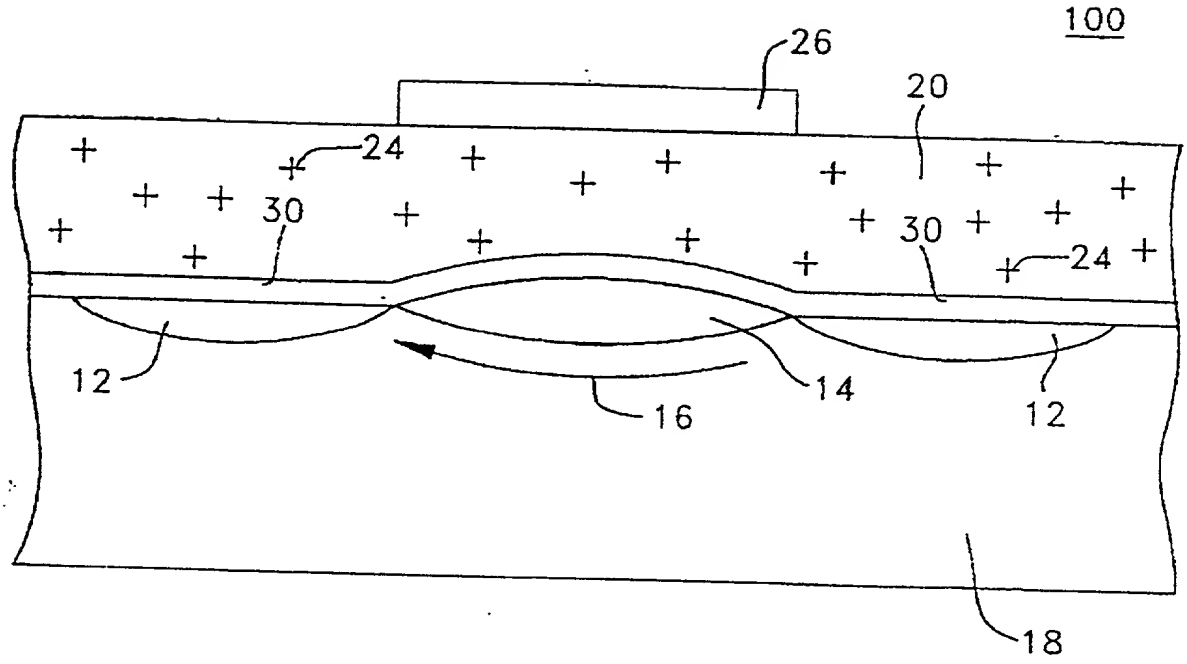

FIG. 3

Atty. Docket No. 94-0302

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS, the specification of which:

Regular or Design Application

__x__ is attached hereto.

____ was filed on _____ as Application Serial No. _____

and was amended on _____ (if applicable).

PCT Application Entering National Phase

____ was filed on _____ as PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of

Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.)	(Filing Date)	(Status-patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Robert C. Podwil (Reg. No. 22,778); W. Scott Railton (Reg. No. 23,039); Arland T. Stein (Reg. No. 25,062); Louis M. Heidelberger (Reg. No. 27,899); Frederick H. Colen (Reg. No. 28,061); Mary E. Buckles (Reg. No. 31,907); Francis M. Linguiti (Reg. No. 32,424); John F. Letchford (Reg. No. 33,328); Daniel H. Golub (Reg. No. 33,701); Gene A. Tabachnick (Reg. No. 33,801); Stanley D. Ference III (Reg. No. 33,879); Kevin J. Garber (Reg. No. 34,171); Gregory L. Bradley (Reg. No. 34,299); John W. Goldschmidt (Reg. No. 34,828); Kent E. Baldauf, Jr. (Reg. No. 36,082); Maria N. Rullo (Reg. No. 37,433); Cheryl L. Gastineau (Reg. No. 39,469), W. Bryan Farney (Reg. No. 32,651) and Lia M. Pappas (Reg. No. 34,095).

Address all telephone calls to Frank M. Linguiti at telephone number (215) 851-8264.

Address all correspondence to
Sylvia A. Ransom
REED SMITH SHAW & McCLAY
P.O. Box 2009
Pittsburgh, PA 15230

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Signature	Randhir P. S. Thakur Date 12/14/95
Full name of sole or first inventor	THAKUR, Randhir P.S.
Residence	Boise, Idaho
Citizenship	India
Post Office Address	3545 S. Bridgeport Place, Boise, ID 83706

Inventor's Signature	Ravi Iyer Date 12/14/95
Full name of second inventor	IYER, Ravi
Residence	Boise, Idaho
Citizenship	India
Post Office Address	5600 Fuchsia, Boise, ID 83705

Name and signature of third inventor on page 3.

Inventor's Signature Howard E. Rhodes Date 12/14/95
Full name of third inventor RHODES, Howard
Residence Boise, Idaho
Citizenship U.S.A.
Post Office Address 631 E. Ridgefield Dr., Boise, ID 83706

REED SMITH SHAW & McCLAY
P.O. Box 2009
Pittsburgh, PA 15230
(412) 288-3131

rev. 6/1995

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Randhir Thakur, Ravi Iyer, and Howard Rhodes

Serial No.:

Filed: August 31, 2000

For: A METHOD TO AVOID THRESHOLD VOLTAGE SHIFT IN THICKER DIELECTRIC FILMS

§ Atty. Docket: 94-0302.02

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DATE OF DEPOSIT 8-31-00

I HEREBY CERTIFY THAT THIS PAPER IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 C.F.R § 1.10 ON THE DATE INDICATED ABOVE AND IS ADDRESSED TO THE ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

Signature

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment recorded in the United States Patent and Trademark Office as set forth below or filed herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor(s).

The Assignee hereby revokes any previous Powers of Attorney and appoints: Charles B. Brantley, II, Reg. No. 38,086; Michael L. Lynch, Reg. No. 30,871; Walter D. Fields, Reg. No. 37,130; Kevin D. Martin, Reg. No. 37,882; and David J. Paul, Reg. No. 34,692 as its attorney or agent, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., referenced below, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

Assignment:

__Filed concurrently herewith for recording, a copy of which is attached hereto.

_X_ Previously recorded on: _12/26/95_, at Reel: 7823 , Frame: 0164

Please direct all communications as follows:

Charles B. Brantley, Mail Stop 525
MICRON TECHNOLOGY, INC.
8000 S. Federal Way
Boise, ID 83716-9632
(208) 368-4557

ASSIGNEE: MICRON TECHNOLOGY, INC.

Date: 8-30-00

By:

Michael L. Lynch, Reg. No. 30,871
Chief Patent Counsel